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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,621	06/07/2000	Sara Ruhina Biyabani	004860.P2438	8620

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EXAMINER	
CASCHERA, ANTONIO A	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/589,621	BIYABANI, SARA RUHINA	
	Examiner	Art Unit	
	Antonio A. Caschera	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9,11-14,16-21 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9,11-14,16-21 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 2-8, 11-14, 16-21 and 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Stortz (U.S. Patent 5,900,885).

In reference to claims 2, 11, 16 and 23, Stortz discloses a video memory architecture including a system memory controller connected via a bus to a system memory, a CPU and to a video buffer in video memory (see Figure 1 of Stortz, System Memory Controller (#15) connects to CPU (#12), memory (#14) via bus (#18) along with video DRAM (#22) and Figure 2, #14, #22, #42a and #42b). Stortz discloses assigning an incremental video buffer in main memory and a dedicated video buffer in video memory (see Figure 2, #42a, 42b and column 2, lines 41-44). Note, the Office interprets the incremental video buffer in main memory functionally equivalent to the frame-preparation memory and dedicated video buffer functionally equivalent to the refresh memory of Applicant's claims. Stortz explicitly discloses using the system memory controller to control both incremental video buffer in main memory and the video buffer in video memory (see column 1, lines 61-64 and column 3, lines 13-16). Note, with Stortz explicitly disclosing the system memory controller coupled to CPU (#12 of Figure 1), main

memory (#14) and video memory (#22) along with the controlling of both main memory and video memory by the system memory controller therefore allows the Office to interpret that Stortz manages the use of the main memory between a graphics subsystem (video controller #20 of Figure 1) and a processing unit (CPU #12 of Figure 1). Further, Stortz explicitly discloses that the allocation of main memory to an incremental video buffer is performed by a modification of the system memory controller (see column 2, lines 54-57), therefore the Office interprets that the system memory controller of Stortz is "operable" for partitioning an address space for the color buffer (since video buffers are used in Stortz, they inherently comprise of color data and are therefore interpreted as equivalent to "color buffers"). Stortz also discloses connecting the incremental video buffer to a graphics subsystem and connecting the video buffer to a display device (see column 1, lines 44-53, column 3, lines 2-6, Figure 1, Memory (#14) is connected to Video Controller (#20) via bus (#18) and DRAM (#22) is connected to Display (#24) and see Figure 2, reference #42a, #42b). Further, the Office interprets that since Stortz discloses that a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see column 3, lines 2-6, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44), the incremental video buffer operates based upon a frame rate and the dedicated video buffer inherently operates upon a refresh rate so that the memory and display devices are compatible. Further since a "portion" of data is written to/and from these memories to a display device along with the fact that Stortz explicitly discloses "video" memories, the Office interprets that such a "portion" refers to a frame of data.

In reference to claim 3, Stortz discloses all of the claim limitations as applied to claim 2 above. Stortz discloses that a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see column 3, lines 2-6, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44).

In reference to claims 4, 13, 17 and 25, Stortz discloses all of the claim limitations as applied to claims 3, 11, 16 and 23 respectively above in addition, the Office interprets that the system memory controller of Stortz inherently copies data from the incremental video buffer, in main memory to the dedicated video buffer in the graphics subsystem at "pre-determined intervals" since "portions" of data are copied at a time and "portions" of data are sent to a display from the video memory. In other words, such a broad term, "pre-determined intervals" is inherently found in the double-buffering techniques of Stortz at each time a new "portion" of video data is required to be displayed.

In reference to claims 5, 12, 18 and 24, Stortz discloses all of the claim limitations as applied to claims 3, 11, 16 and 23 respectively above. The Office interprets that since Stortz discloses that a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see column 3, lines 2-6, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44), the incremental video buffer operates based upon a frame rate and therefore copies data when an entire frame is ready for further processing/display. Even further support for Office's interpretation can be found in column 1, lines 15-27 of Stortz

wherein an explanation of frame buffer data organization is disclosed thereby further suggesting that such buffers in Stortz do operate upon video frames.

In reference to claims 6, 14 and 19, Stortz discloses all of the claim limitations as applied to claims 1, 11 and 16 respectively above. Stortz discloses a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see columns 2-3, lines 67-12, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44). Note, the Office interprets the third-logical buffer of Applicant's claims equivalent to the look-ahead buffer of Stortz.

In reference to claims 7 and 20, Stortz discloses all of the claim limitations as applied to claim 6 and 19 respectively above. Stortz discloses that a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see columns 2-3, lines 67-12, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44). Stortz further discloses that the next portion of data is read directly from the look-ahead buffer, instead of system memory, and received by the dedicated video buffer (see column 3, lines 6-8). Therefore, the Office interprets Stortz discloses such "disconnection" of the system memory from the graphics subsystem as the role of the look-ahead buffer is switched to the frame-preparation memory (previously known as the incremental video buffer located in system memory).

In reference to claims 8 and 21, Stortz discloses all of the claim limitations as applied to claims 7 and 20 respectively above. The Office interprets that since Stortz discloses that a

portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see column 3, lines 2-8, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44), the incremental video buffer operates based upon a frame rate and therefore copies data when an entire frame is ready for further processing/display. Stortz explicitly discloses, "After this local data is read, the next portion of display data is read directly from look-ahead video buffer..." (see column 3, lines 6-8). Even further support for Office's interpretation can be found in column 1, lines 15-27 of Stortz wherein an explanation of frame buffer data organization is disclosed thereby further suggesting that such buffers in Stortz do operate upon video frames.

In reference to claim 26, Stortz discloses all of the claim limitations as applied to claim 23 above. Claim 26 is equivalent in scope to the combination of claims 5-8 and is therefore rejected under similar rationale.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stortz (U.S. Patent 5,900,885) in view of Akeley (U.S. Patent 6,075,543).

In reference to claim 9, Stortz discloses all of the claim limitations as applied to claim 2 above. Stortz does not explicitly disclose the system memory controller switching the designations of the buffers so that the currently designated incremental video buffer now becomes the refresh memory and is now connected to the display device however Akeley does. Akeley discloses a system and method for managing multiple frame buffers (see column 3, lines 29-30). Akeley explicitly discloses executing an OpenGL Swap command whereby the current contents of a Back Buffer become the new contents of a Front Buffer, swapping the roles of the buffers (see columns 4-5, lines 64-6) and therefore swapping the connection of the Front Buffer to the Back Buffer contents connected with the display device (see Figure 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the buffer management techniques of Akeley with the teachings of Stortz in order to implement a double buffering memory system which doesn't suffer from the problems of latency between data transfers of multiple buffers (see column 2, lines 16-29 of Akeley) by creating efficient data transfers while maximizing CPU cycles.

Response to Arguments

3. Applicant's arguments, see pages 2-4 of Applicant's Remarks, filed 09/06/06, with respect to the rejection(s) of claim(s) 2-9, 11-14, 16-21 and 23-26 under 35 USC 103(a), in view of Priem et al. and Rao, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Stortz and Akeley.

4. Note, the Office acknowledges the previous use of the Stortz reference in rejecting previous versions of the claims of the current application at hand and herein responds to previous arguments made by Applicant, in view of the Stortz reference. Further, the reintroduction of the Stortz reference by the Office is in response to Applicant's recently filed claim language whereby the claims have been rewritten to be deficient of the, "unified" term in the phrase, "unified memory architecture," therefore allowing the Stortz reference to be reapplied in claim rejections.

Applicant's arguments dated 02/10/03, respond to a rejection based upon the Stortz reference (see pages 12-15 of Applicant's Remarks). Applicant argues that the Stortz reference does not teach a unified memory architecture (see pages 12-13, last 4 lines thru line 1 of Applicant's Remarks). This argument is seen as moot since Applicant's amendments to the claim language have omitted such limitation of a unified memory architecture. Further, Applicant argues that Stortz's video processor/controller does not manage the use of main/system memory between a graphics subsystem and another processing unit (see page 13, lines 1-4 of Applicant's Remarks). The Office points out that it now relies upon the system memory controller of Stortz, instead of the video controller, to read upon the managing of system memory between a graphics subsystem and a processing unit limitation of the claims (see above rejection of claim 1, for example). In particular, Stortz explicitly discloses using the system memory controller to control both incremental video buffer in main memory and the video buffer in video memory (see column 1, lines 61-64 and column 3, lines 13-16 of Stortz). Therefore the Office interprets Stortz to disclose a sole memory controller...managing the use of the main memory between a graphics subsystem and a processing unit.

Applicant's arguments dated 07/03/03, respond to a rejection based upon the Stortz reference (see pages 8-10 of Applicant's Remarks). Applicant argues that the Stortz reference does not teach or suggest that the portion of system memory can be re-allocated to the system memory controller and therefore teaches using two different components to control memory in the system (see page 8 of Applicant's Remarks). The Office points out that it now relies upon the system memory controller of Stortz, instead of the video controller, to read upon the managing of system memory between a graphics subsystem and a processing unit limitation of the claims (see above rejection of claim 1, for example). In particular, Stortz explicitly discloses using the system memory controller to control both incremental video buffer in main memory and the video buffer in video memory (see column 1, lines 61-64 and column 3, lines 13-16 of Stortz). Therefore in response to the above arguments, Stortz explicitly discloses using only one or a sole memory controller (system memory controller) to control memory in the system (i.e. both system memory and video memory). Further, Applicant indicates that the Office had previously interpreted Stortz to not disclose partitioning an address space for the color buffer into two logical buffers...one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory (see page 9, last paragraph of Applicant's Remarks). The Office points out that it now interprets the incremental video buffer in main memory functionally equivalent to the frame-preparation memory and dedicated video buffer functionally equivalent to the refresh memory of Applicant's claims. Further, Stortz explicitly discloses that the allocation of main memory to an incremental video buffer is performed by a modification of the system memory controller (see column 2, lines 54-57 of Stortz), therefore the Office interprets that the system memory controller of Stortz is "operable" for partitioning an address space for the color buffer

(since video buffers are used in Stortz, they inherently comprise of color data and are therefore interpreted as equivalent to "color buffers"). Therefore the Office applies Stortz as a prior art reference in the above rejection of the current claims.

Applicant's arguments, filed in the Appeal Brief dated 03/03/04, respond to a rejection based upon the Stortz reference (see page 5 of the Appeal Brief) and are similar to the arguments as indicated above and therefore are addressed in a similar manner.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (571) 272-7781. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung, can be reached at (571) 272-7794.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

571-273-8300 (Central Fax)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (571) 272-2600.

aac

PATENT EXAMINER
11/16/06

KEE M. TUNG
SUPERVISORY PATENT EXAMINER